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MOSFET Scaling Crisis and the Evolution of Nanoelectronic Devices: The Need for Paradigm Shift in Electronics Engineering Education

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Abstract

This paper briefly discusses the development of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) scaling and its crisis and the evolution of the new nanoelectronic devices and their potential applications both in analog and digital circuits. The paper also discusses the need to introduce nanoelectronic devices education in the electrical engineering curricula in the Gulf Cooperation Countries (GCC).

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1. Introduction

At present there is a great concern that the scaling down of MOSFETs is approaching its limits. Researchers around the world are trying to develop new devices in order to continue increasing the speed of operation and the packaging density of integrated circuits. Eventually the classical MOSFET structure will disappear and new devices with new structures using new materials will be introduced. The major intention of this paper is to present a brief description about the current and recent developments in MOSFET scaling and the new emerging devices and their potential application in both analog and digital circuits. The paper will also discuss the

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challenges of introducing nanotechnology education in the curricula of the electrical engineering departments in the GCC countries.

2. MOSFET Scaling Down From 10um to 32nm [1]

When developed in 1960, the channel length of the MOSFET was around 10μ. Today most of the integrated circuits utilize CMOS technology with channel length around 40 nm. Scaling down has the following advantages:

- With smaller transistors and shorter interconnects more circuits can be fabricated on each silicon wafer. This leads to cheaper circuits.
- Smaller transistors and shorter interconnects lead to smaller capacitances and higher IC speed.
- Smaller transistors lead to reduced power supply voltages and power consumption.
- Without scaling doing the job of a single PC microprocessor chip (operating a billion transistors at 2 GHz) using 1970 technology would require the power output of an electrical power generation plant.

However, scaling down has its own problems. At very short gate length the major constraints which dominate the whole design are:

- The static and dynamic power consumption.
- Overheating and possible evaporation become major concerns.
- Increased electric filed within the oxide and increased leakage gate-current.
- The classical physics do not apply, available MOSFET models cannot be used and quantum effects need to be employed for modeling device characteristics. Electrons, in quantum mechanics, are represented by traveling waves. Electrons at a potential barrier that is higher than the electron energy become decaying functions. As the barrier thickness decreases the tunneling probability increases.

2.1. Scaling Around 90nm (gate length 37/65 nm) strained silicon

Scaling around 90nm became possible by using the strained silicon technology. In this technology the hole surface mobility of a PFET can be raised when the channel is compressively stressed.

Strained silicon is a layer of silicon in which the silicon atoms are stretched beyond their normal inter-atomic distance. This can be accomplished by putting the layer of silicon over a substrate of Silicon Germanium (SiGe). As the atoms in the silicon layer align with the atoms of the underlying SiGe layer (which are arranged a little farther apart, with respect to those of a bulk silicon crystal), the links between the silicon atoms become stretched - thereby leading to strained silicon. Moving these silicon atoms farther apart reduces the atomic forces that interfere with the movement of electrons through the transistors and thus better mobility resulting in better chip performance and lower energy consumption. These electrons can move 70% faster allowing strained silicon transistors to switch 35% faster.

More recent methods of inducing strain include doping the source and drain with lattice atoms such as germanium and carbon. Germanium doping of up to 20% in the PMOS source and drain causes uniaxial compressive strain in the channel, increasing hole mobility. Carbon doping as low as 0.25% in the NMOS source and drain causes uniaxial tensile strain in the channel, increasing electron mobility. Covering the NMOS transistor with a highly stressed silicon nitride layer is another way to create uniaxial tensile strain.

2.2. Scaling Around 65nm (gate length 37/65 nm)

SiO2 has been the preferred gate insulator since silicon MOSFET's beginning. Over the years the oxide thickness has been reduced from 300 nm for the 10 um technology to 1.2 nm for the 65 nm technology). Thinner oxide raises the current and hence the speed. Manufacturing thin oxide is not easy. If the oxide is too thin, the electric field in the oxide can be so high as to cause destructive breakdown. For Silicon-Dioxide (SiO2) films

thinner than 1.5 nm, tunneling leakage gate current becomes serious. At 1.2 nm, SiO2 leaks 1000A/cm^2. If an IC chip contains 1mm^2 total area of this thin dielectric, the chip oxide leakage current would be 10 A. The leakage current can be reduced by a factor of 10 with the addition of nitrogen into SiO2.

2.3. Scaling Around 45nm (gate length 22/37 nm) High-k Dielectric Materials/Metal Gates

Alternatively high-k dielectric materials can replace SiO2. Zirconium Dioxide (ZrO2), Aluminium Oxide (Al2O3) and Hafnium Oxide (HfO2) have relative dielectric constants higher than SiO2. For example a 6 nm thick HfO2 film is equivalent to a 1 nm SiO2 in the sense that both films give the same value of Cox and hence the channel current. But with thicker oxide film the leakage gate current is several orders of magnitude less than in SiO2 films.

On the other hand, initially, the gate of MOSFET was typically made of metals such as Al. After 1970, heavily doped highly conductive polycrystalline silicon (poly-Si) has been the standard gate material because of its ability to withstand high temperatures without reacting with SiO2. The depletion in the semi metallic poly-Si adds "dielectric thickness" to the true SiO2, thus, increasing oxide thickness. Because of the high carrier density in metals, depletion effect is negligible. Hence the use of metals is preferred. After 2008, the trend is to introduce metal gates and replace SiO2 by high-k material.

2.4. Scaling Around 32nm (gate length 16/25 nm) Wet Lithography

Optical Lithography is the process by which oxide can be selectively removed from specific areas. With a photoresist, deep ultraviolet light and reduction optical lenses, different patterns can be printed. Because of the difficulty of finding suitable materials for lenses and masks at wavelength shorter than 193 nm, wet lithography is used to print the fine patterns. In wet lithography the gap between the lens and the wafer is filled with water. When the light enters the water its wavelength is reduced thus improving the resolution. Other liquids with higher refractive index can be used to improve the resolution.

2.5. Scaling Around 22nm (gate length 13/20 nm): New Structures (FinFET)

These structures allow gate length scaling beyond the limit of conventional MOSFET. As the oxide thickness decreases the gate gets perfect control on the channel- but only right at the Si surface. As the channel length is reduced, drain to channel distance is reduced. The drain may have more control than the gate along paths that are some distance below the Si surface where the gate is very far away and its control is weak.

With Vgs < Vt, an N-channel MOSFET is in the off state. However, a leakage current can still flow between the drain and the source causing a serious power consumption issue even in standby operation. Typically it is required to maximize the gate-to-channel capacitance and to minimize the drain-to-channel capacitance. This would reduce drain leakage current. As the channel length is reduced, the drain-to-source and the drain-to-channel distance is reduced and the influence of the drain will increase. Even with tiny oxide thicknesses the gate will have perfect control on the Si surface but deep in the channel the drain will have more control, causing leakage paths under the surface. To eliminate deep submerged leakage, it is required to give the gate more control over the channel. This can be achieved by providing gate control from more than one side of the channel. The Si film is made so thin that no leakage path is far from one of the gates. With more than one gate this structure is called multigate MOSFET or sometimes FinFET.

2.6. Scaling Below 102nm (gate length 13/20 nm)

Below 10nm scaling down is possible but becomes difficult and costly. According to the International Roadmap for Semiconductors (ITRS) there is a consensus among researchers that CMOS devices will stop scaling by 2020. Some of the emerging promising technologies that have potential to replace the current generation of CMOS, for ultimate scaling down, are: Carbon Nanotubes (CNTs), Single Electron Transistors (SETs) and Organic Filed Effect Transistors (OFETs). These alternatives form a complete new branch of science namely nanoelectronics.

3. Nanoelectronic Devices: Carbon Nanotubes (CNTs) [2]

CNTs are new form of carbon with unique electrical and mechanical properties. Nanotubes can be smaller than 1 nm in diameter and are made of one-molecule-thick sheets of graphite that roll up to form the tube. They may be composed of a single shell-single wall (SWNTs) or several shells-several walls (MWNTs). Depending on the folding angle and the diameter of the tube, nanotubes can be metallic or semiconducting. The electrical conductivity of metallic nanotube can exceed that of the best metals. The transconductance and mobility of semiconducting nanotube can exceed that of the best semiconductors. Nanotube's environment may affect whether it is truly metallic or not. Semiconducting nanotubes can work as field-effect transistor (CNTFET) with the gate switching the tube on when it is negative and off when it is positive. Operating frequencies up to 2.6 GHz have been reported. Nanotube diodes are also available.

3.1. Applications of Carbon Nanotubes

Fabricated and tested a Single Wall CNTFET-based radio receiver including resonant antennas, fixed RF amplifiers, RF mixers, and AF amplifiers. Eight authors from departments of: Physics, Materials Science and Engineering, Electrical and Computer Engineering and Chemistry. Carbon nanotube transistor arrays for multi-stage complementary logic and ring oscillators and logic circuits with carbon nanotube transistors are also available. CNT-based MEMS piezoresistive gas sensors, CNT-based detectors of polar molecules and a three dimensional thermal sensor based on single-walled carbon nanotubes are available.

3.2. Hybrid CMOS and CNT on Chip

Integration of nanostructures with CMOS circuitry results in:

- Reduced parasitic due to absence of wire bonding.
- Low-cost miniaturized system-on-chip (or system-on-package) solutions.
- Higher sensitivities through on-chip signal processing. Unfortunately, this is not an easy task as the high CNT growth temperatures (~700 C) are not compatible with CMOS technology. Recently, the fabrication of a 44 kΩ SWCNT resistor onto an OA fabricated using 0.5um CMOS process was reported.

4. Nanoelectronic Devices: Single Electron Transistor (SET) [3]

The operation of SET is based on the behavior of small conducting particles surrounded by insulating material. These particles are called islands. Because of its size, an island can be charged only by a small number of electrons. Because of the insulating layer that surrounds the island, the transport of electrons to and from the island is possible only by tunneling effect. Thus, the voltage of each island can take only quantized values.

A SET is formed of a drain, source, gate and an island. Its operation is similar to that of MOSFET except that electron conduction takes place one electron at a time while in MOSFET many electrons simultaneously take part in the conduction. By applying the proper gate voltage, the potential energy of the conduction island is made low enough to allow one electron from the source to tunnel to the conduction island. With the potential energy of the drain lower than that of the conduction island, the electron then tunnels to the other side to reach the drain. With the conduction island empty and the potential lower again, the process repeats.

The SET fabrication process in Silicon is CMOS-compatible. The use of SETs combined with MOS transistors allows a compact realization of basic logic functions that exhibit periodic transfer characteristics. These basic SET logic gates are useful for implementing binary logic circuits, multi-valued (MV) logic circuits and binary-MV-mixed logic circuits in a highly flexible manner. SET-based radio-frequency mixers, SET-based charge sensors, RF-SET ultrasensitive electrometers applicable in scientific instrumentation, metrology, and nanoelectromechanical (NEM) systems are also available.

5. Nanoelectronic Devices: Organic Field Effect Transistor (OFET)

An organic field-effect transistor (OFET) is a field effect transistor using an organic semiconductor in its channel. OFETs can be prepared either by vacuum evaporation of small molecules, by solution-casting of polymers or small molecules, or by mechanical transfer of a peeled single-crystalline organic layer onto a substrate. These devices have been developed to realize low-cost, large-area electronic products. OFETs have been fabricated with various device geometries. The most commonly used device geometry is bottom gate with top drain- and source electrodes, because this geometry is similar to the thin-film silicon transistor (TFT) using thermally grown Si/SiO_2 oxide as gate dielectric. Organic polymers, such as poly(methyl-methacrylate) (PMMA), can be used as dielectric, too.

Recently, the first full-color, video-rate, flexible, all plastic display in which both the thin film transistors and the light emitting pixels were made of organic materials.

6. Nanoelectronic Devices: Circuit Modeling

As in the case of the conventional CMOS circuit design, the modeling of devices and the simulation of the circuit would be a key step to design nano-electronic circuits. In SPICE it is assumed that:

- the current/voltage characteristic of a device is only a function of its size.
- the current/voltage characteristic of a device is affected by neighboring devices only through the changes of the terminal voltages of those devices.
- no quantum mechanical effects are taken into consideration.

This is not the case for nano-devices particularly for the SET.

7. Nanoelectronic Devices: Education

Education in nanoelectronic devices is, therefore, extremely important. It presents a major challenge for existing educators and curriculum developers as it has connections to many academic disciplines. Educators should offer a broad knowledge base for students. The interdisciplinary nature of the various subjects and skills needs to be emphasized. Traditional engineering education, which largely focuses on a particular domain, is no longer adequate for this new nanotechnology era. Nanotechnology will be one of the key research fields in the future, and needs enhanced emphasis/promotion. There is a need to introduce undergraduate and graduate education in the nanoscale science and engineering field. Such education must be capable of providing students with the appropriate nanofabrication and characterization tools, instruments, and capabilities to enable them to understand and develop new circuits and applications using nanoelectronic devices.

8. Conclusion

In the GCC universities, it appears that the introduction of multidisciplinary education is important if we want to have a real contribution and impact on the development of nanoelectronic devices, circuits and systems. The present compartment attitude of engineering departments in GCC universities should come to an end and multidisciplinary education must be introduced both at the graduate and undergraduate levels. Without this we cannot have a real contribution to the advancement of science and technology. As a first step, until multidisciplinary courses are introduced, this author suggests that educators should introduce nanoelectronic devices in their graduate and undergraduate courses. This is essential to prepare students for the future where MOSFET devices will disappear and will be replaced by nanoelectronic devices.

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